

FM1DDR3 I/F

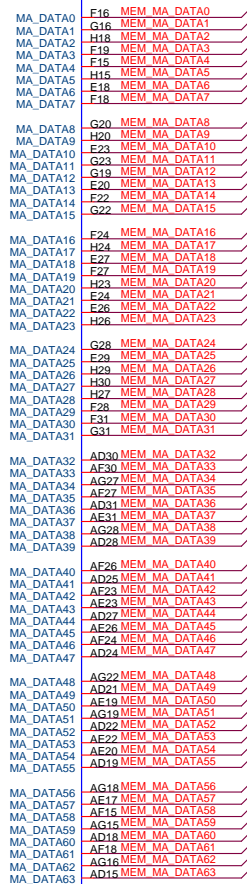
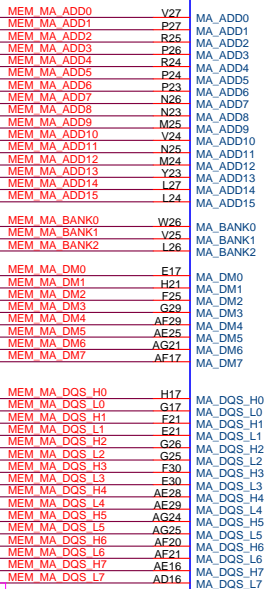
6 MEM_MA_DQS_L[7..0] <-->

6 MEM_MA_DQS_H[7..0] <-->

6 MEM_MA_DM[7..0] <-->

6 MEM_MA_ADD[15..0] <-->

6 MEM_MA_BANK0
6 MEM_MA_BANK1
6 MEM_MA_BANK2



MEM_MA_DATA[63..0] 6

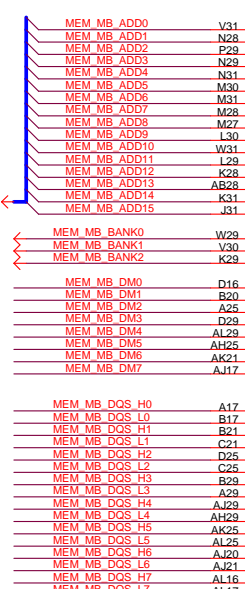
7 MEM_MB_DQS_L[7..0] <-->

7 MEM_MB_DQS_H[7..0] <-->

7 MEM_MB_DM[7..0] <-->

7 MEM_MB_ADD[15..0] <-->

7 MEM_MB_BANK0
7 MEM_MB_BANK1
7 MEM_MB_BANK2



MEM_MB_DATA[63..0] 7

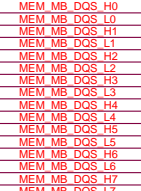
7 MEM_MB_DQS_L[7..0] <-->

7 MEM_MB_DQS_H[7..0] <-->

7 MEM_MB_DM[7..0] <-->

7 MEM_MB_ADD[15..0] <-->

7 MEM_MB_BANK0
7 MEM_MB_BANK1
7 MEM_MB_BANK2

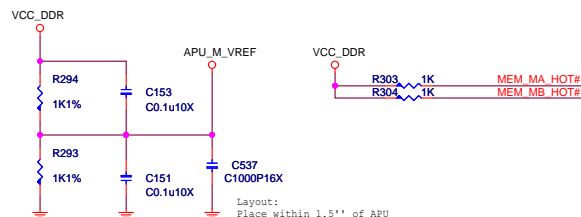


N12-9040020-F02

N12-9040020-F02

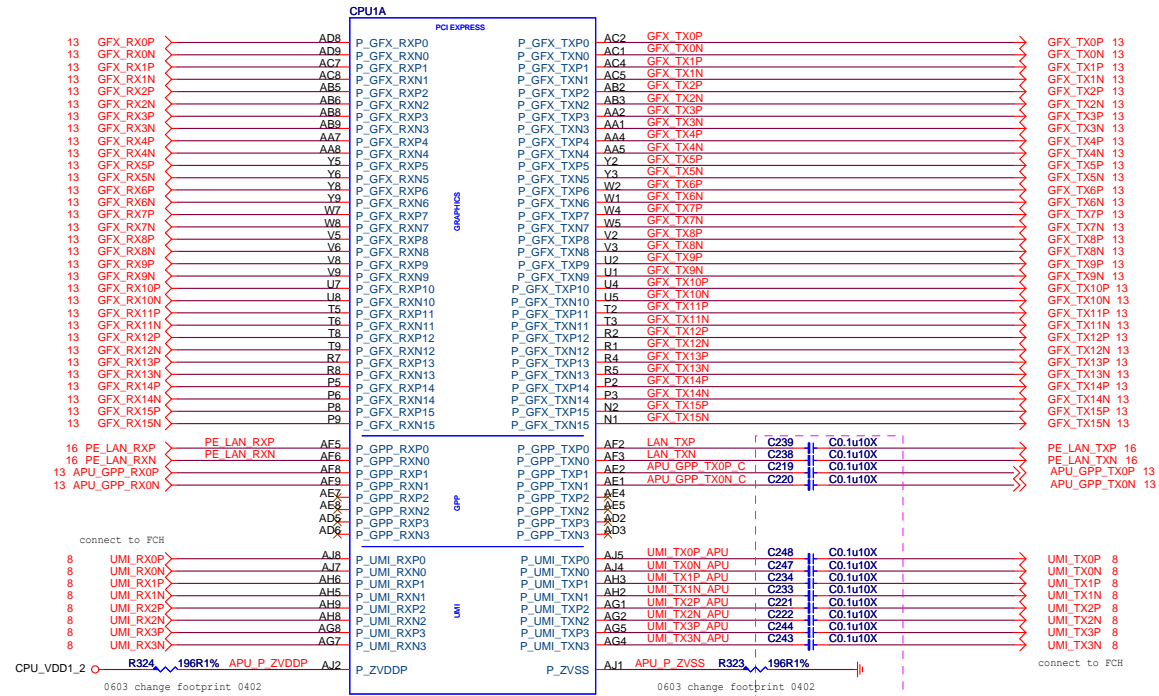
UDIMM A1
MA_CLK_H/L[3] CK1/CK1#
MA_CLK_H/L[0] CK0/CK0#
MA1_CS_L[1:0] S1#:S0#
MA1_ODT[1:0] ODT[1:0]

UDIMM B1
MB_CLK_H/L[3] CK1/CK1#
MB_CLK_H/L[0] CK0/CK0#
MB1_CS_L[1:0] S1#:S0#
MB1_ODT[1:0] ODT[1:0]



Title			
FM2 DDR3 I/F			
Size	Document Number		Rev
Custom	MS-7721		2.3
Date:	Thursday, July 26, 2012	Sheet	2 of 33

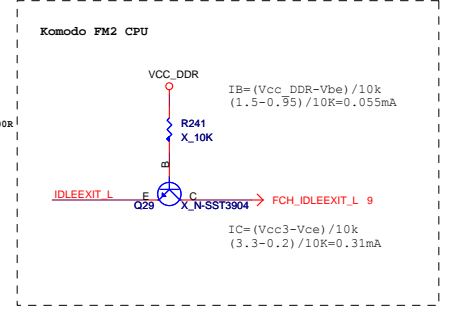
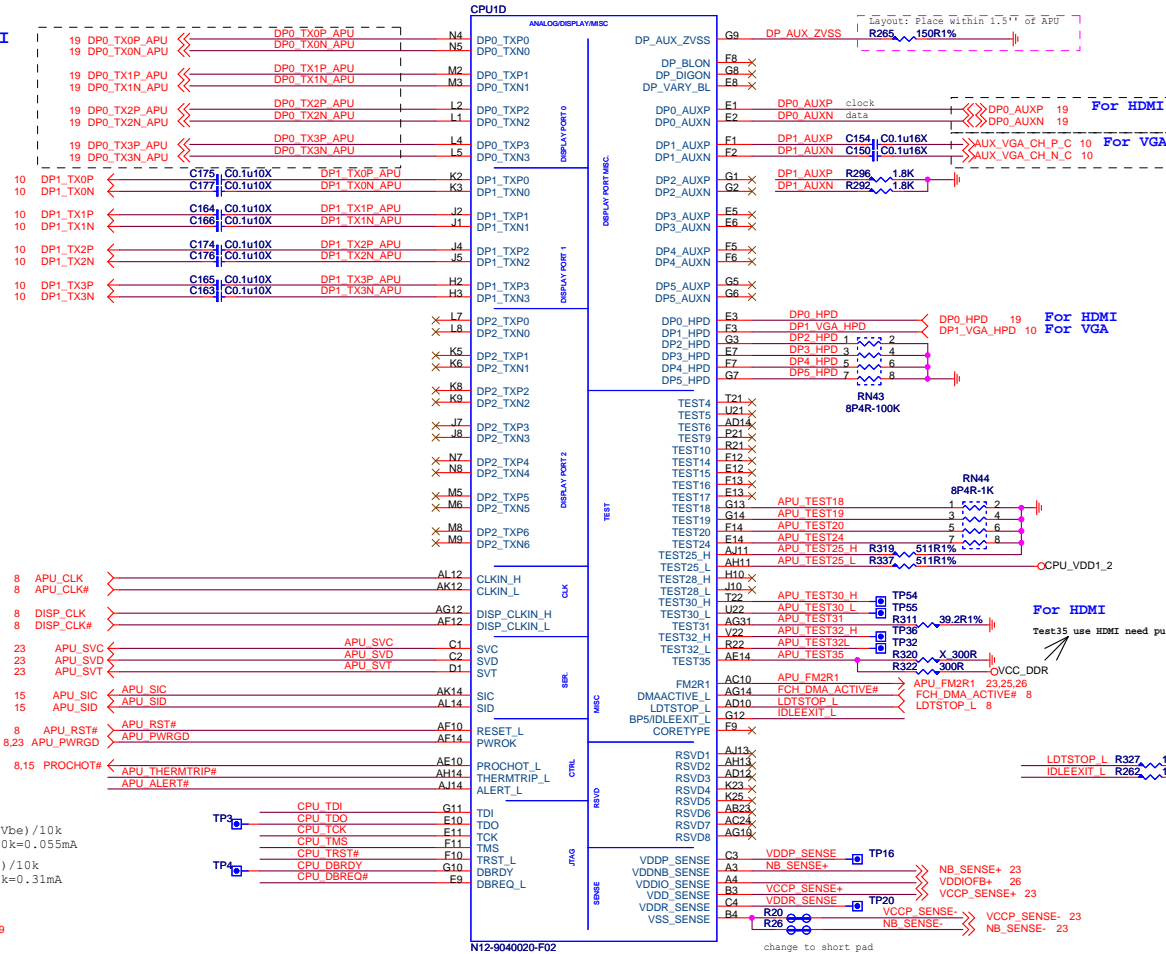
FM2 PCIE I/F



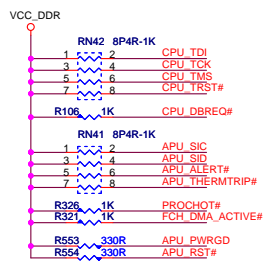
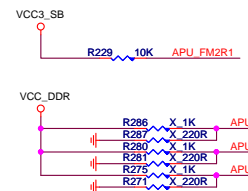
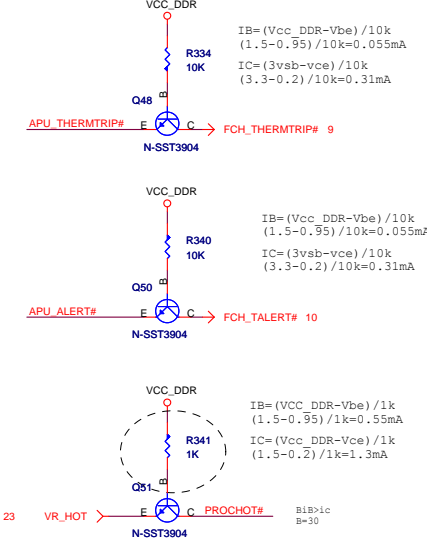
85ohm +/-10%
the CAP need over 500mil from the cpu PIN

For HDMI

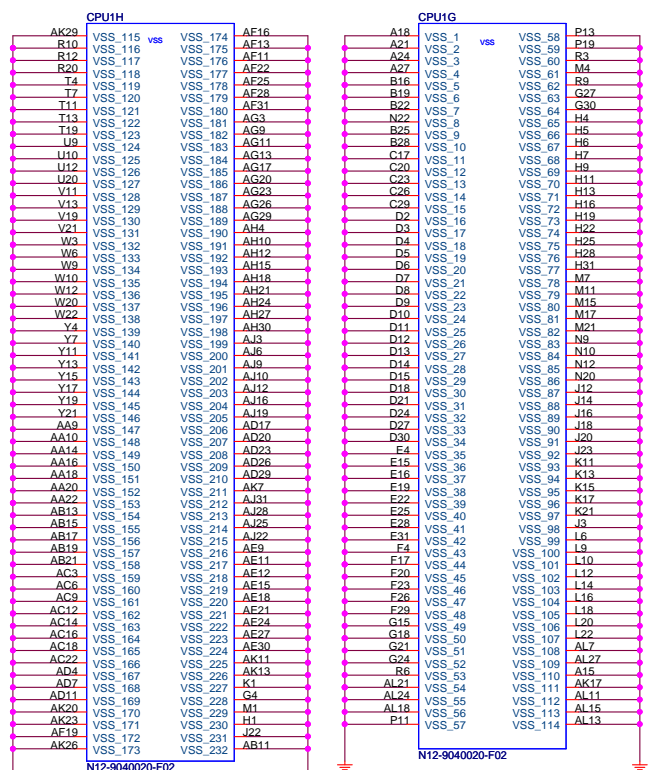
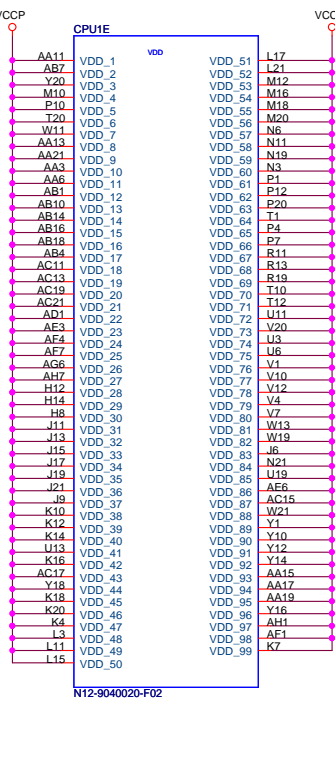
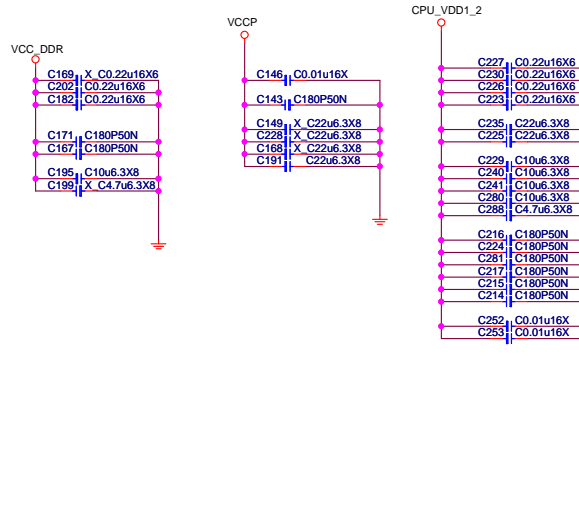
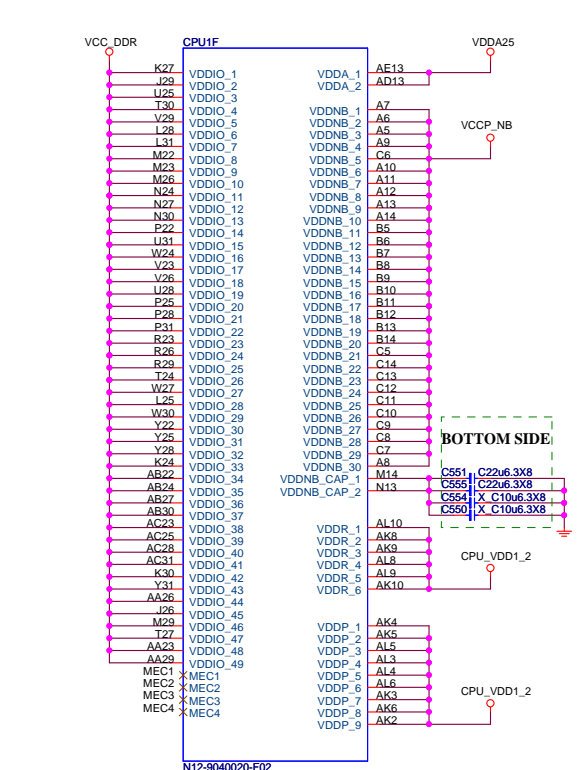
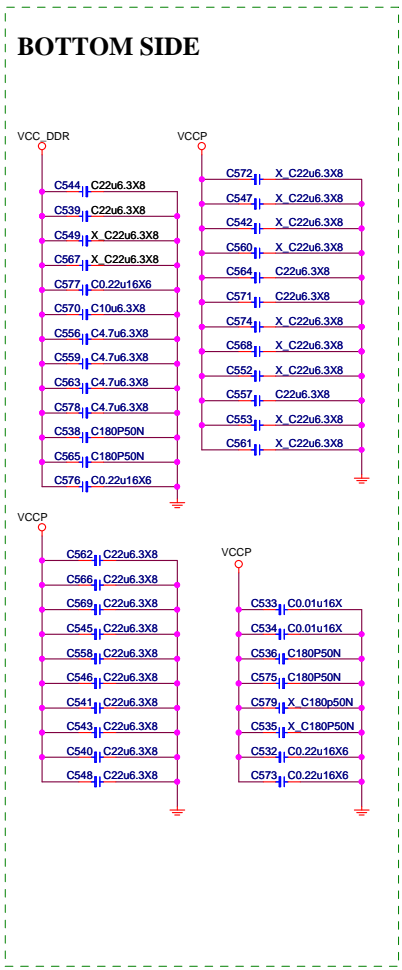
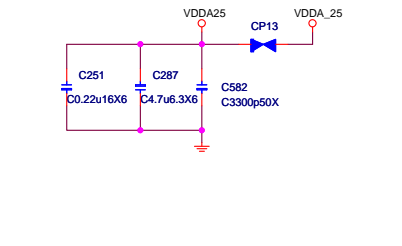
For VGA

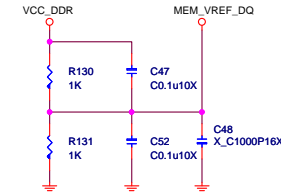
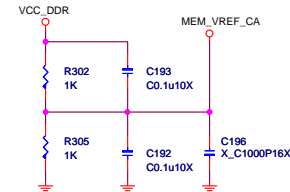
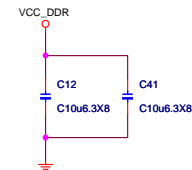
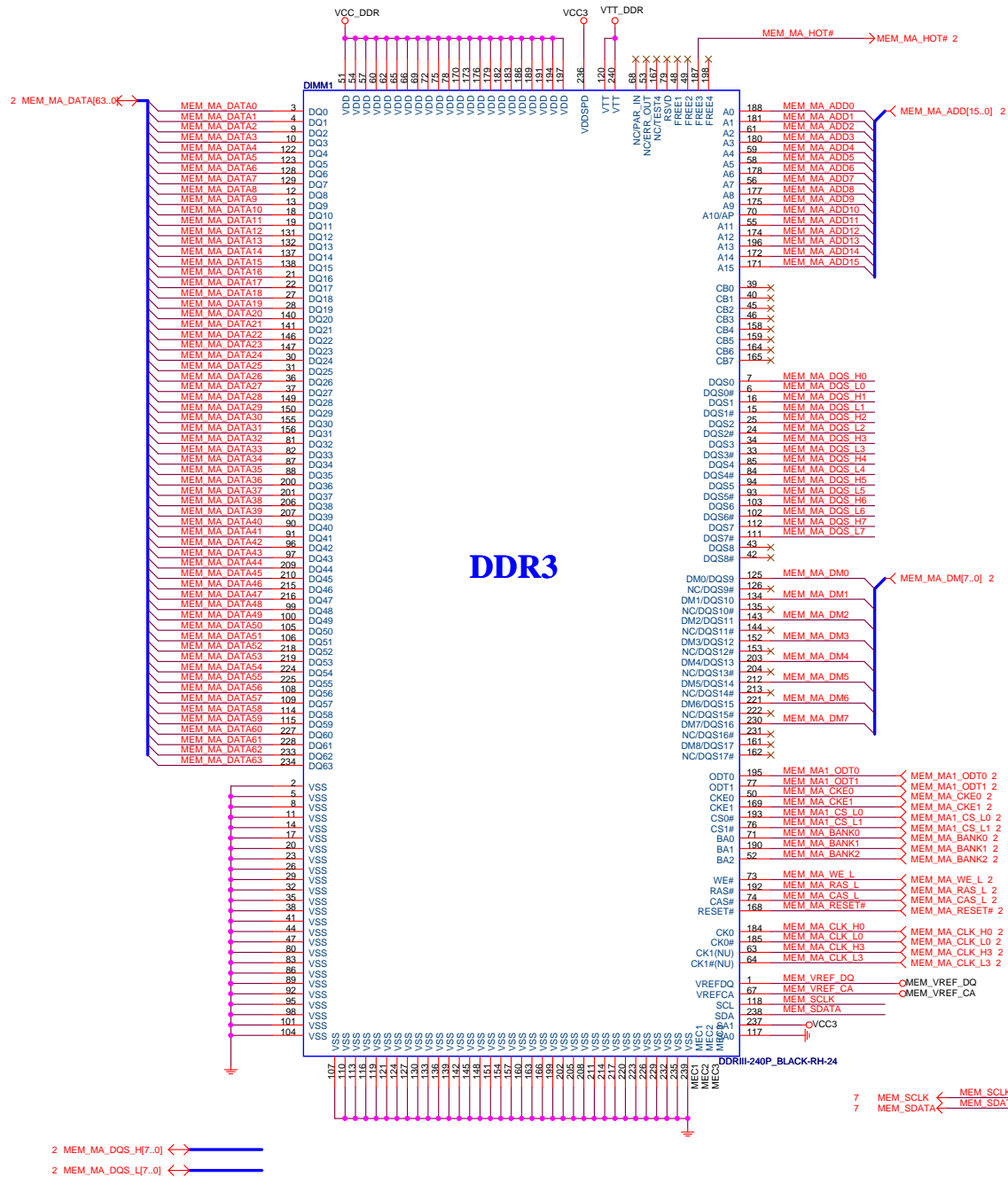


PULL UP



VCC_DDR 5A
VDDA 0.9A
VCCP_NB 41A
CPU_VDD1_2 = VDDR 4A + VDDP 6A
VCCP 60A,90A,110A

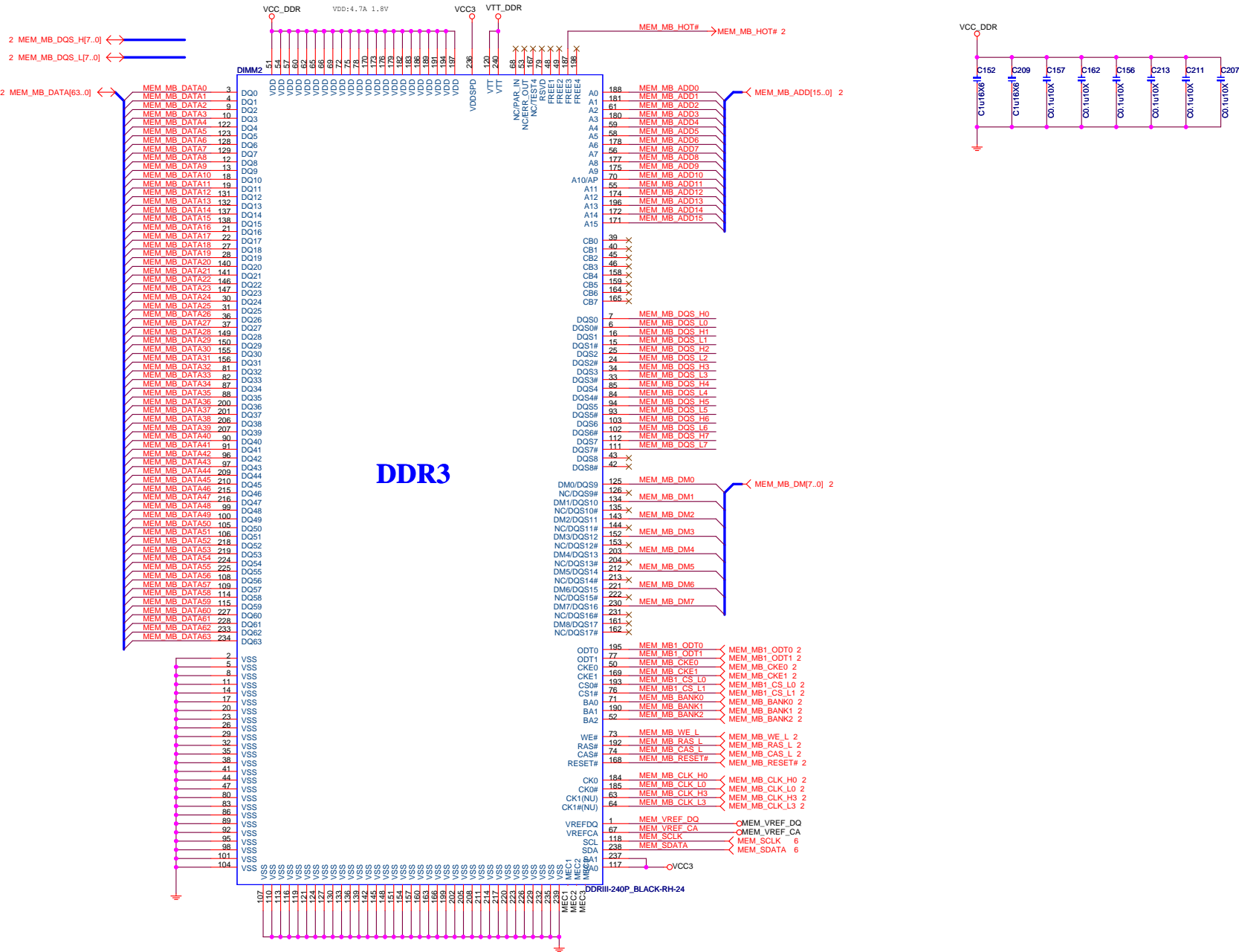




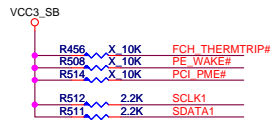
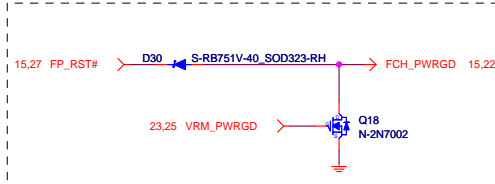
follow circuit checklist suggest value

DDR-III DIMM Config.

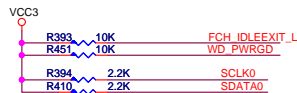
DEVICE	ADDRESS	CLOCK
DIMM 1	10	P/N_DDR1_A
DIMM 2	11	P/N_DDR1_B
DIMM 3	N/A	
DIMM 4	N/A	



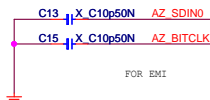
HUDSON ACPI/USB/AZ/GPIO



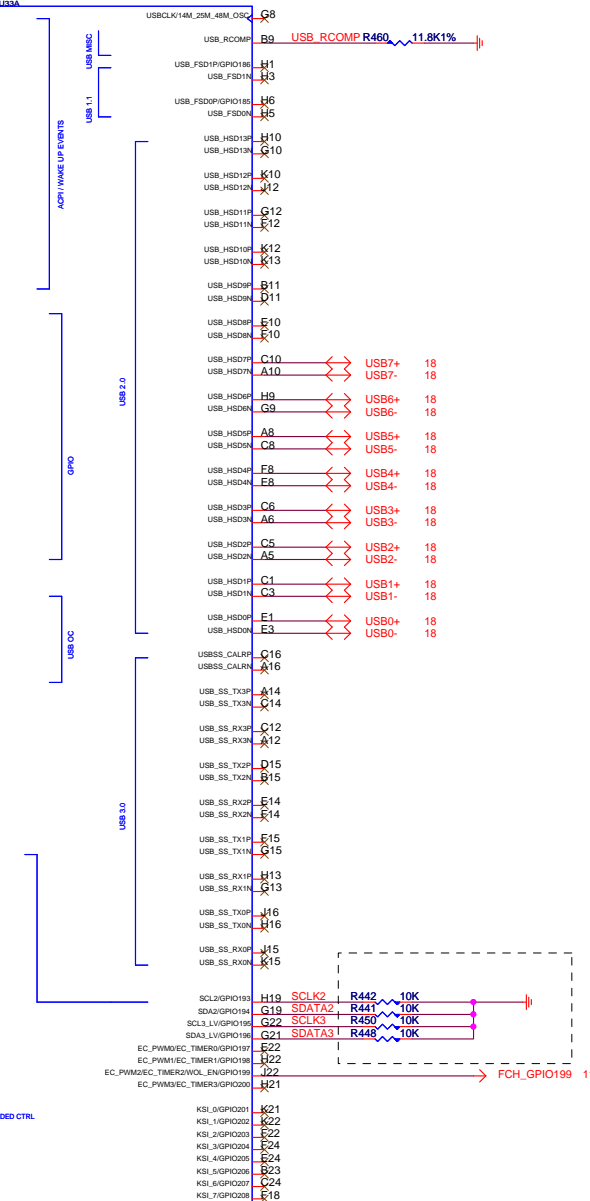
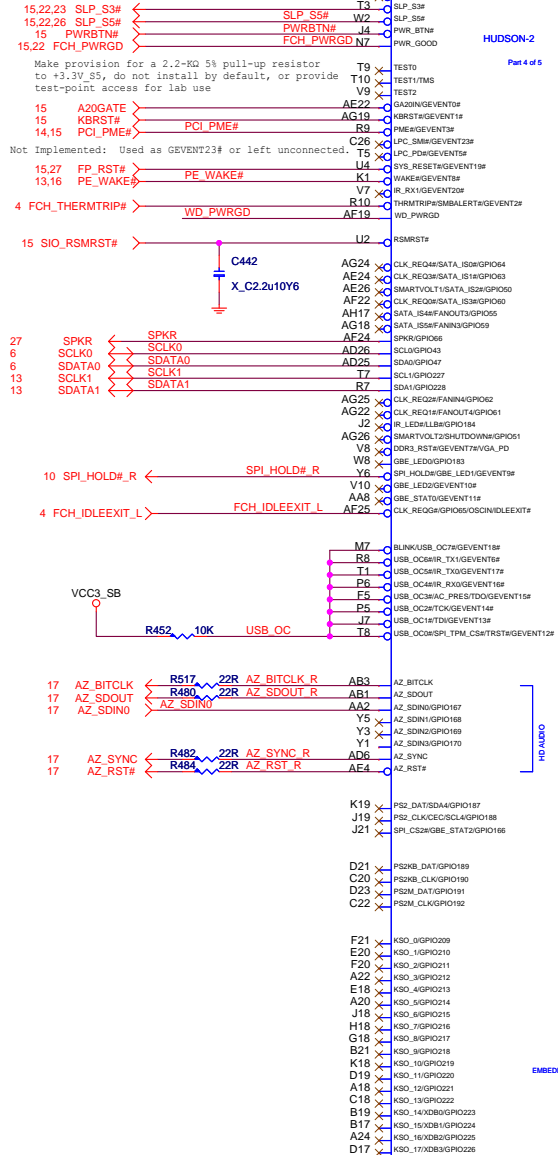
```
S5 POWER DOMAIN
ROUTE TO LAN,PCIE,PCI
```

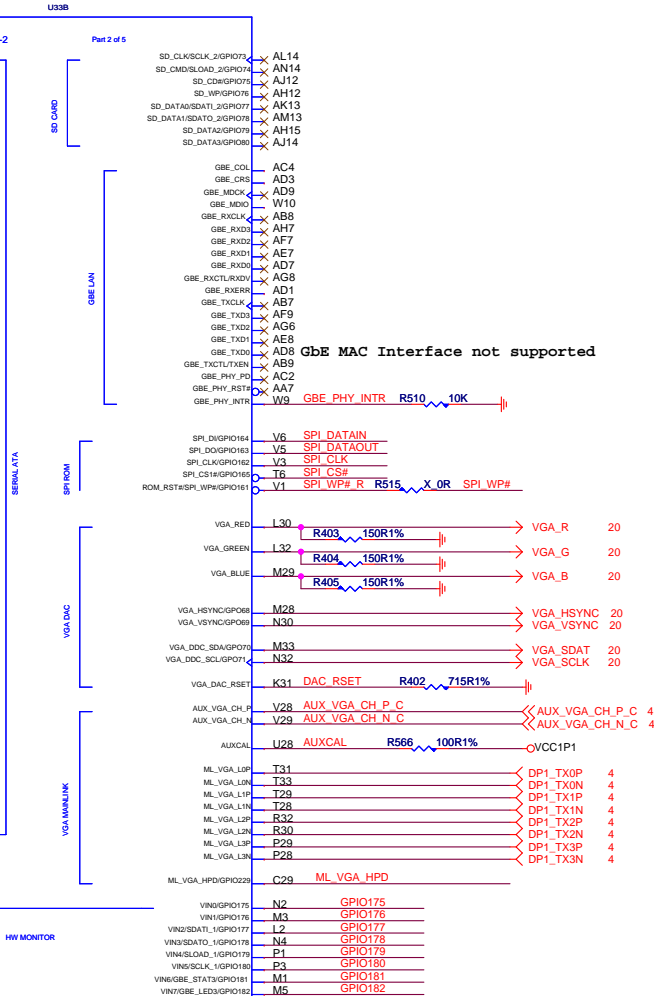
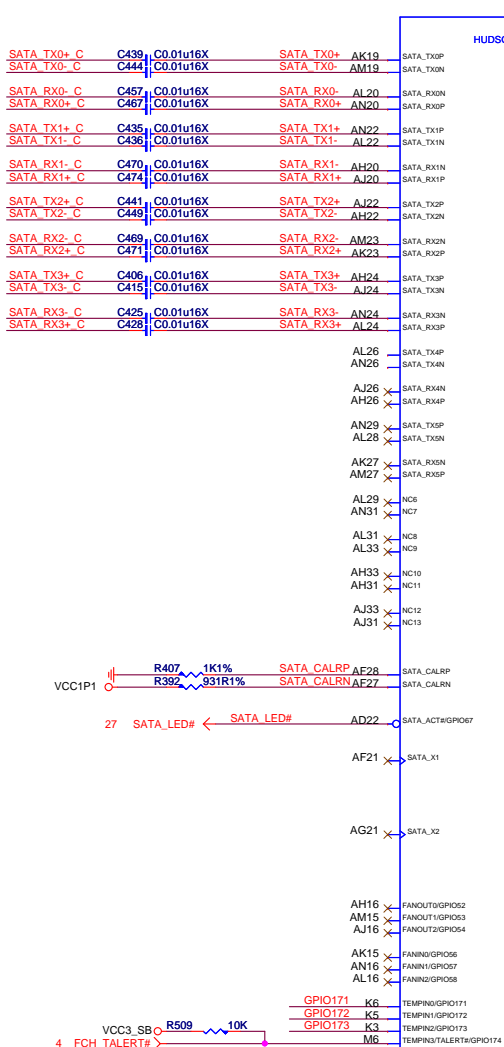
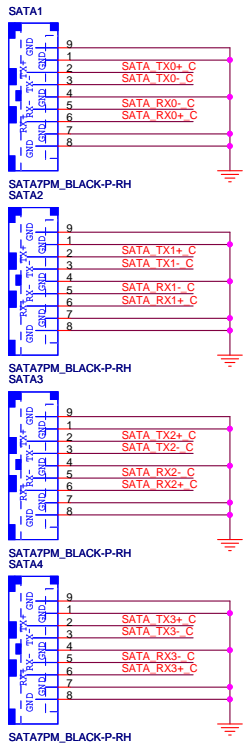


S0 POWER DOMAIN
ROUTE TO DIMMs,CLK Gen,SIO

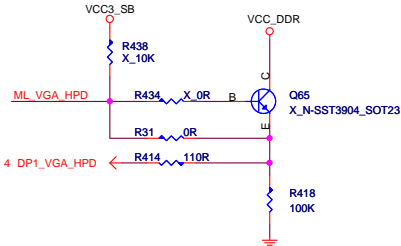


FOR EMI

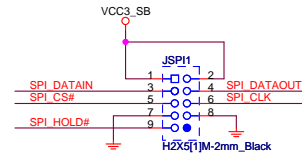
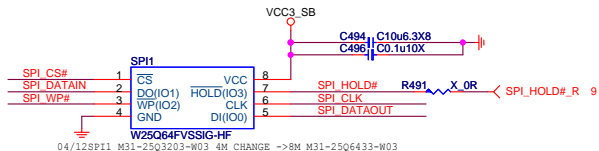




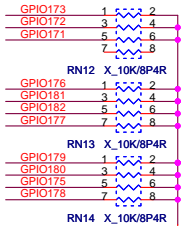
VGA HPD



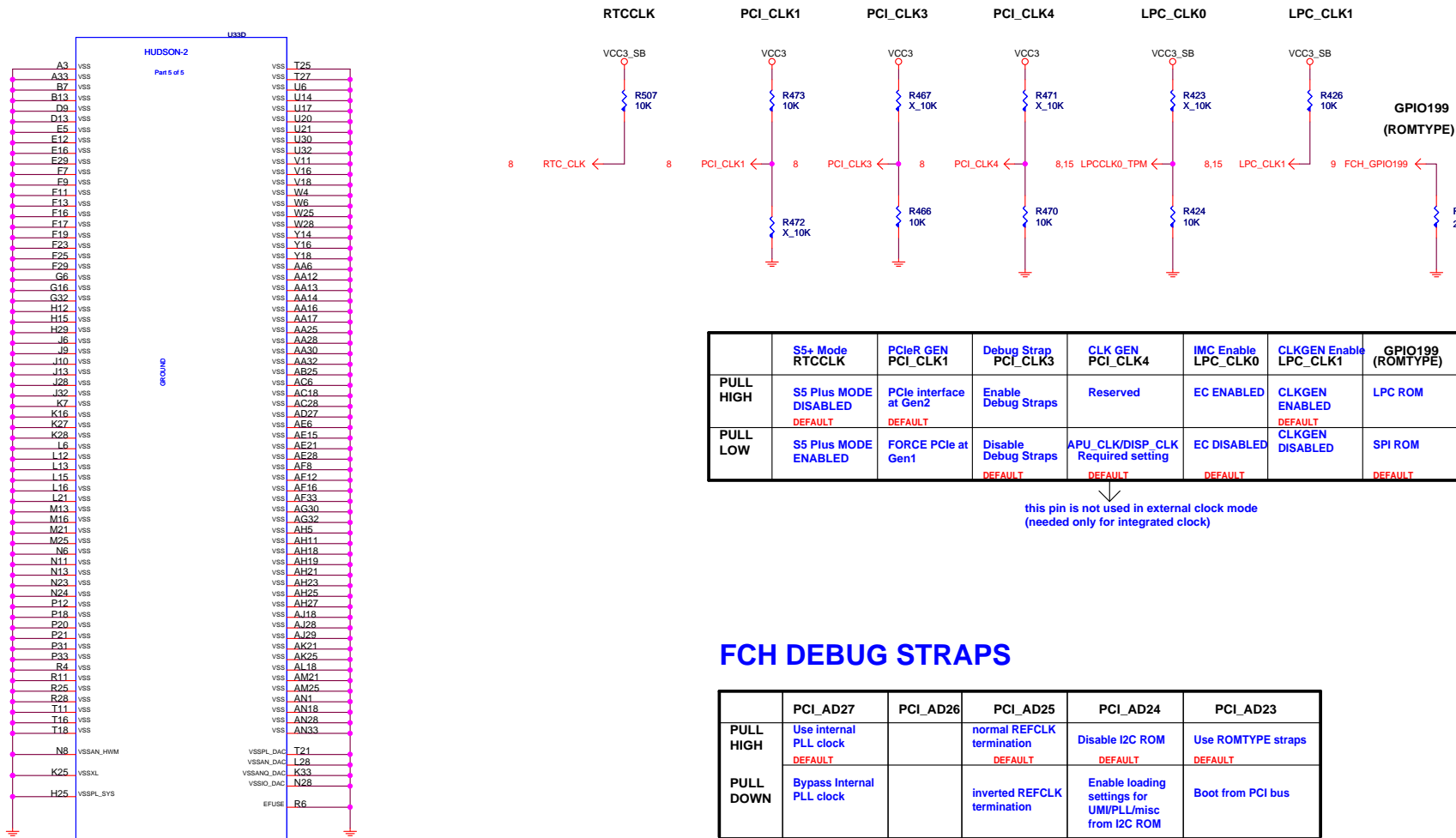
SPI ROM & DEBUG HEADER



Use GPIO 10-KΩ 5% pull-down resistor
Use the other function
10-KΩ 5% pull-up resistor to +3.3V_55



FCH REQUIRED STRAPS

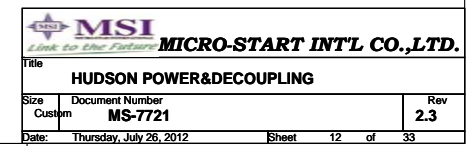


Layout:
VSSPL_SYS,VSSAN_HWM CONNECT TO GND
WITH A SEPERATED VIA

FCH DEBUG STRAPS

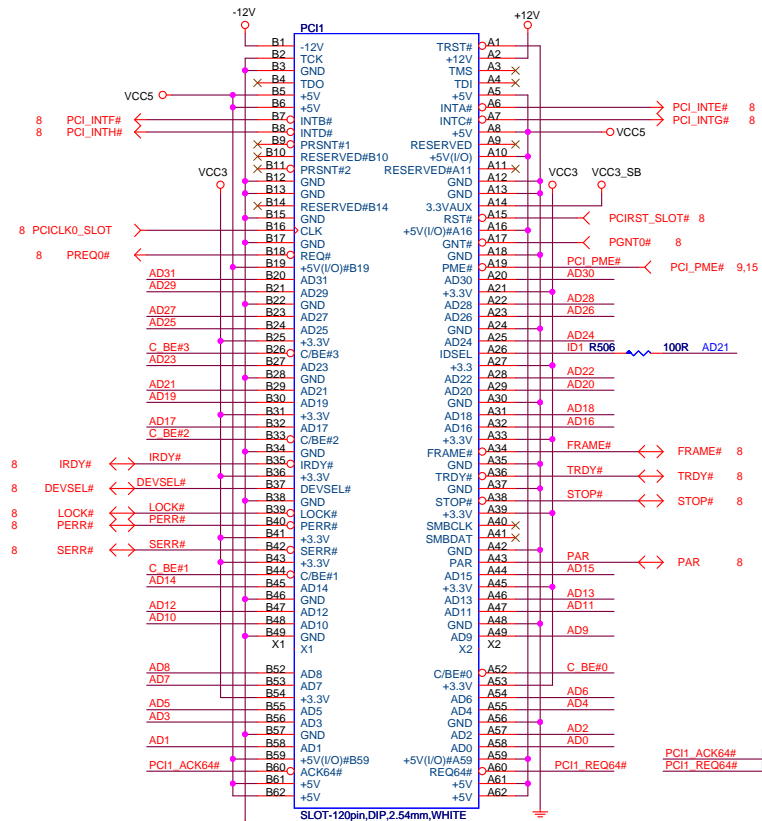
	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
PULL HIGH	Use internal PLL clock DEFAULT		normal REFCLK termination DEFAULT	Disable I2C ROM DEFAULT	Use ROMTYPE straps DEFAULT
PULL DOWN	Bypass Internal PLL clock		inverted REFCLK termination	Enable loading settings for UMV/PLL/misc from I2C ROM	Boot from PCI bus

+1.1V DUAL 454mA



3.3V 7.6A
5V 5.0A
12V 0.5A

PCI SLOT 1 (PCI VER: 2.2 COMPLY)



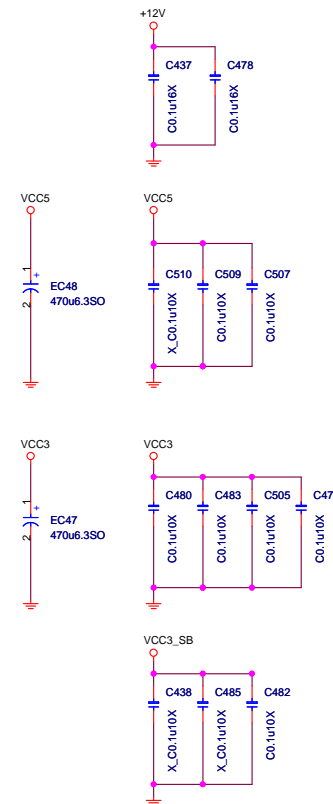
IDSEL = AD21
MASTER = PCI_REQ#0
PCI_GNT#0

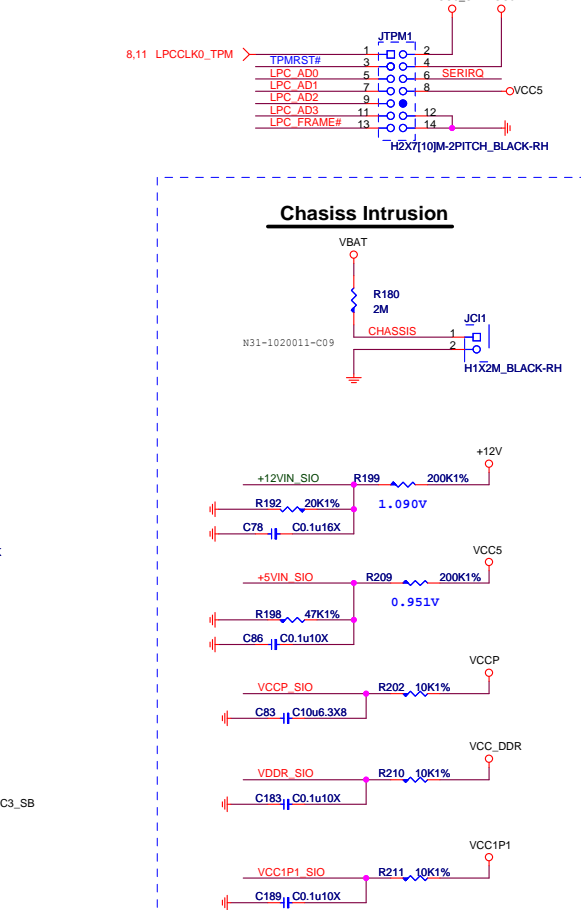
PCI Express X1 slot


+12V	- 1 A
+3.3Vaux (wake)	- 750mA
+3.3Vaux (no wake)	- 40mA
+3.3V	- 6.0A

PCI Config.

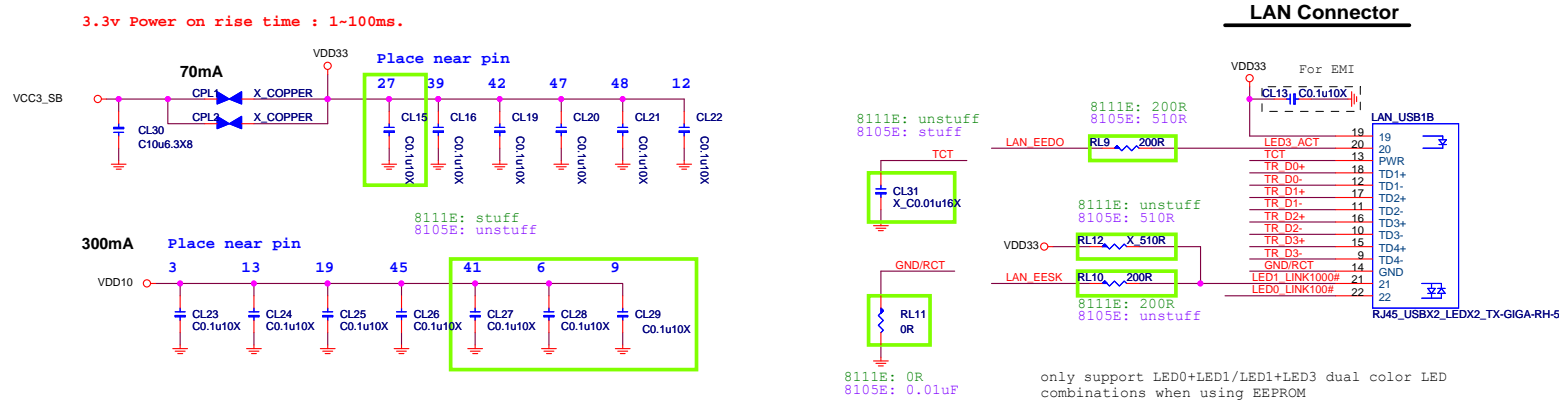
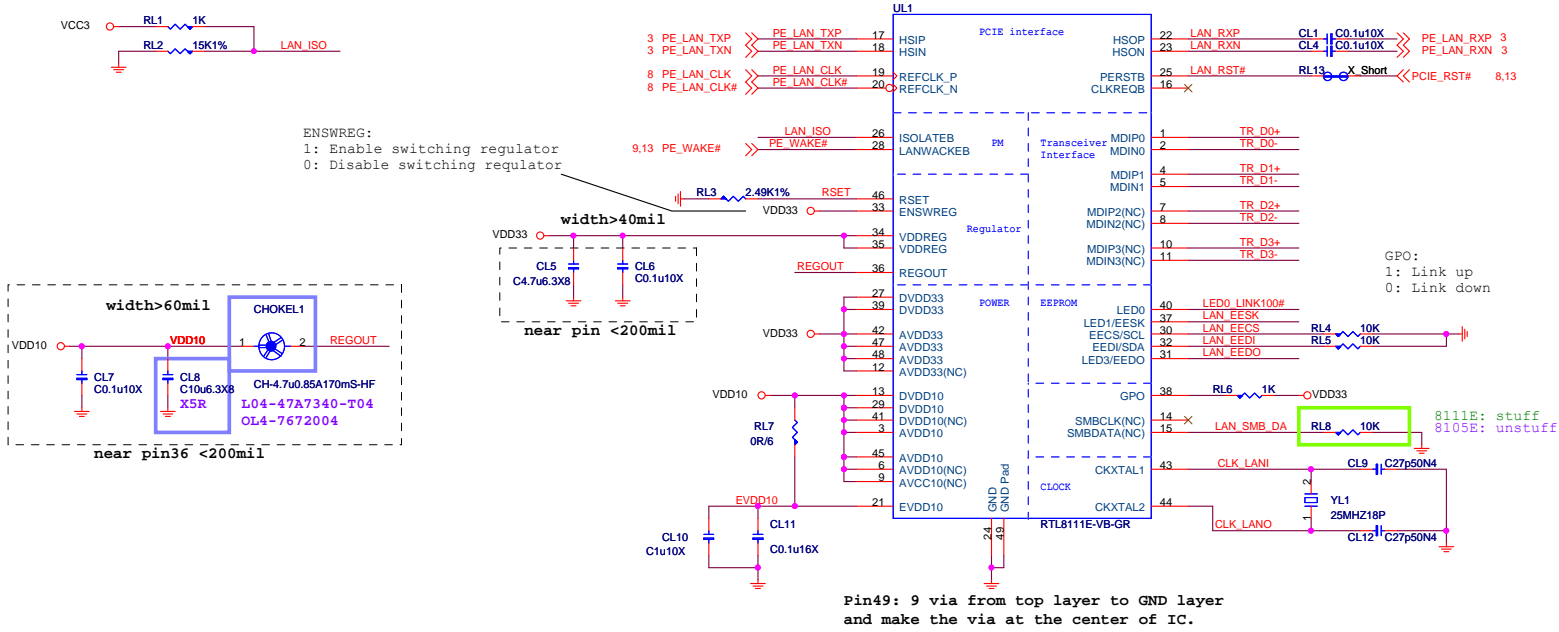
DEVICE	MCP1 INT Pin	REQ# /GNT#	IDSEL	CLOCK
PCI Slot 1	PIRQ#E PIRQ#F PIRQ#G PIRQ#H	PREQ#0 PGNT#0	AD21	CLK_33M_PCH_PCI (ICS113)





 MSI <i>Link to the Future</i>				MICRO-START INT'L CO.,LTD.			
Title SUPER I/O F71869							
Size Custom		Document Number MS-7721				Rev 2.3	
Date: Thursday, July 26, 2012		Sheet 15		of 33			

RTL8111E/8105E



8105E POWER Consumption

	3.3V	mW
10 M Idle/TxRx	14/75	46/248
100 M Idle/TxRx	43/66	142/218
S0 ALDPS	3.2	11

8111E POWER Consumption

	3.3V	mW
10 M Idle/TxRx	12/66	40/218
100 M Idle/TxRx	31/44	102/145
Giga Idle/TxRx	135/163	452/538
ALDPS	4	13

Giga-Lan	10/100-Lan
N58-22F0731 Link Yellow Active Blinking 1000 Orange 100 Green 10 None	N58-22F0771 Link Yellow Active Blinking 1000 Orange 100 Green 10 None
19 20 21 22	19 20 21 22

ALC887-VD
VT1708S CE

11mA

Closed Codec

VCC3

Closed Codec

CA3 C10u6.3X8

CA2 C0.1u10X

VOUT

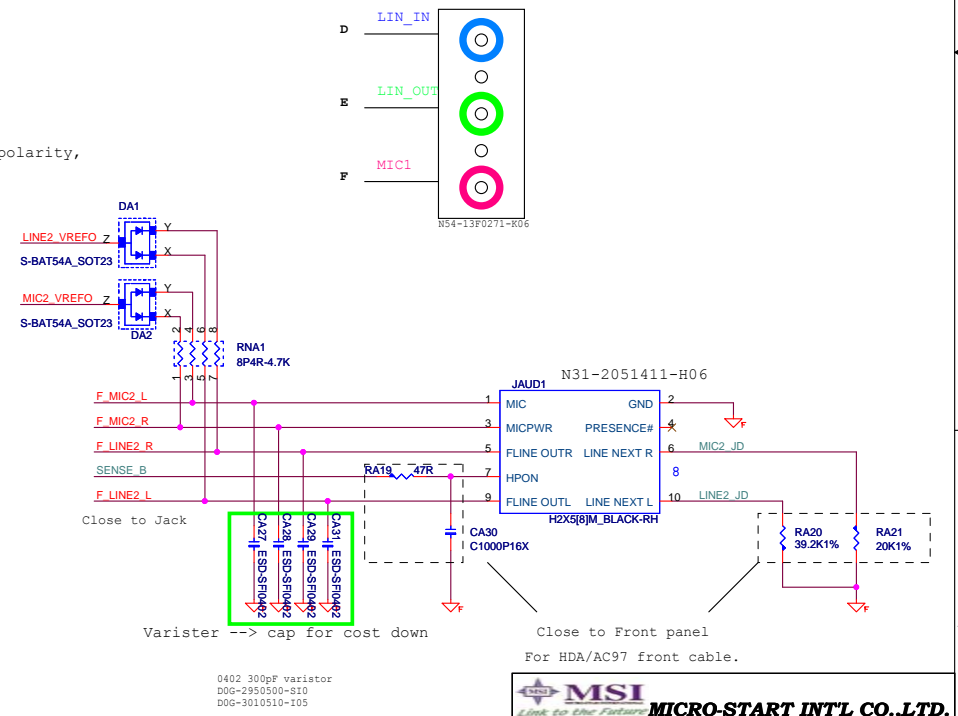
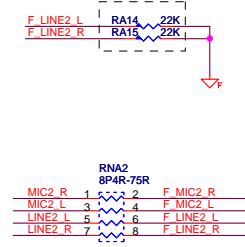
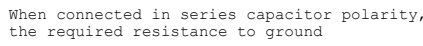
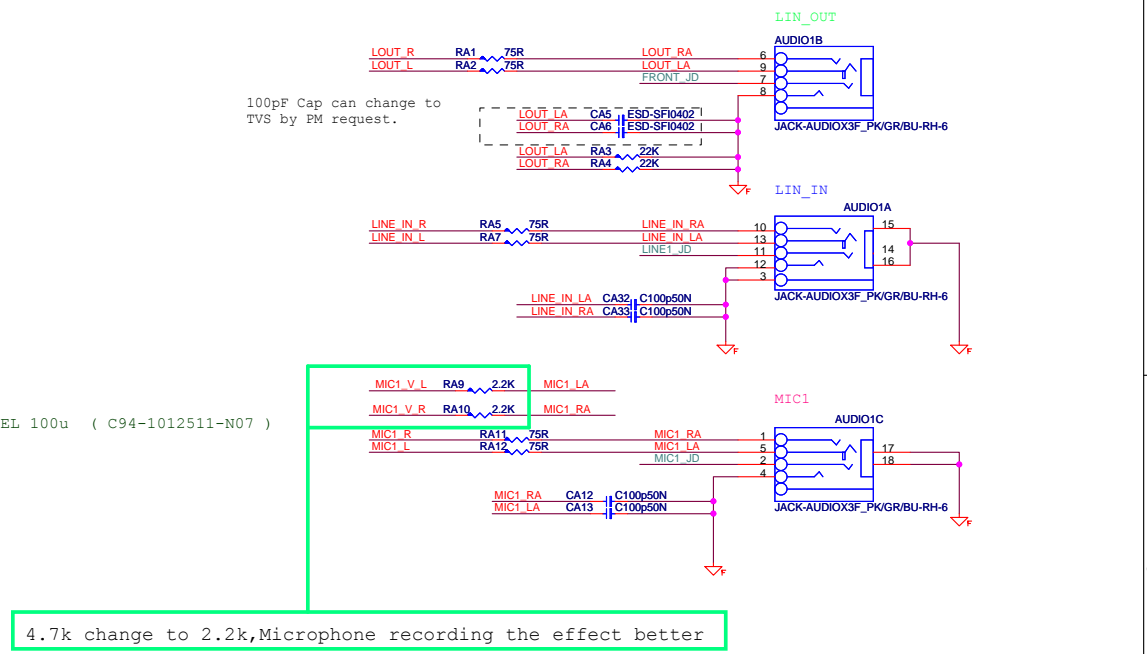
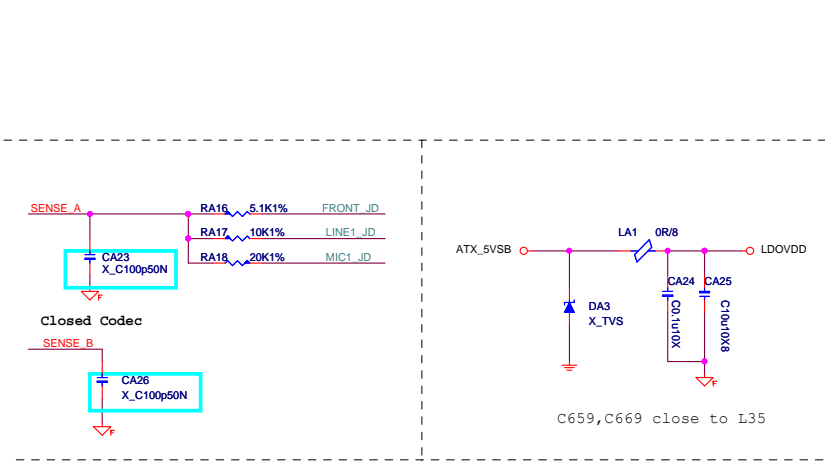
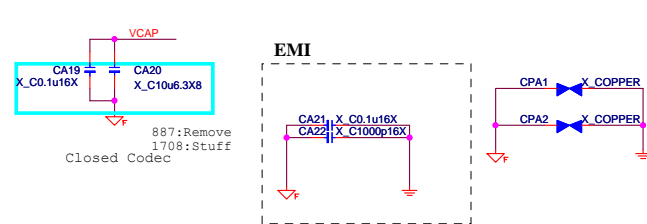
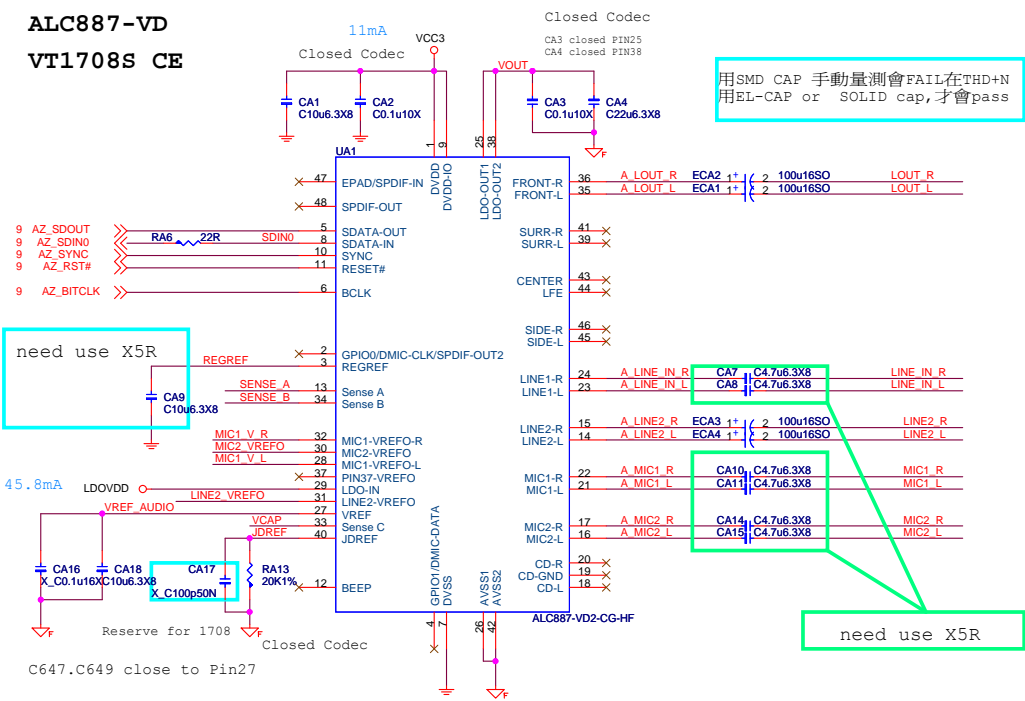
CA3 C0.1u10X

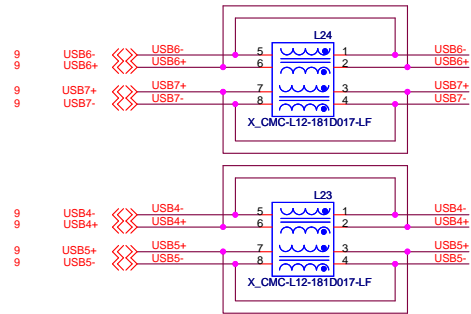
CA4 C22u6.3

Closed Codec

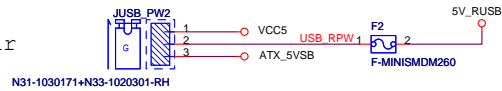
CA3 closed FIN25

CA4 closed FIN38

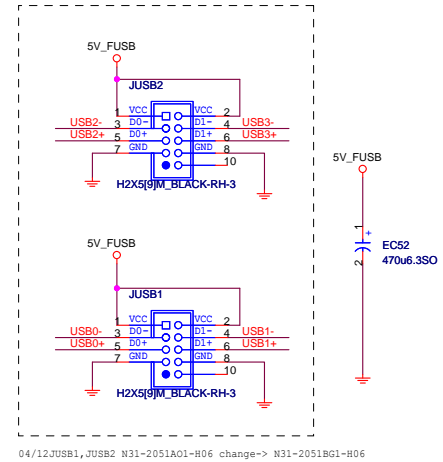
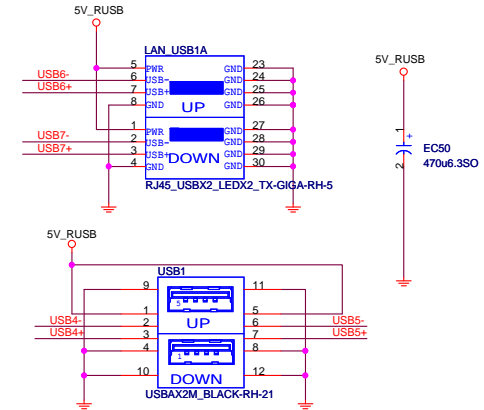
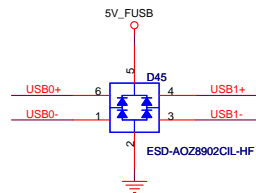
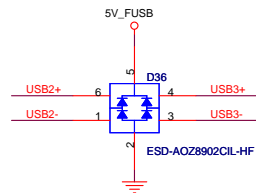
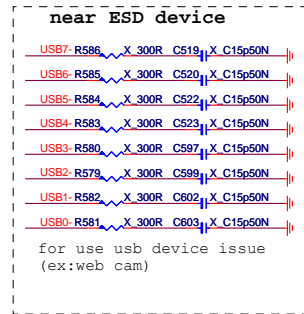
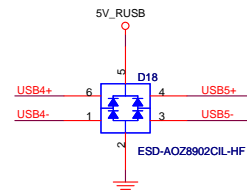
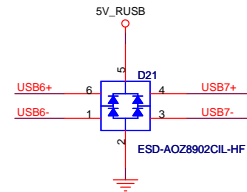
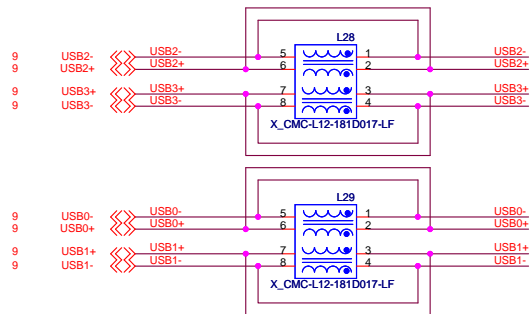
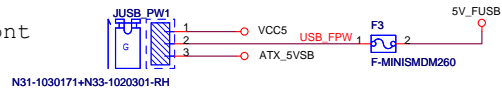




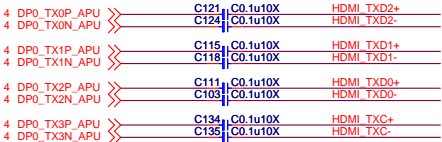
Near Rear



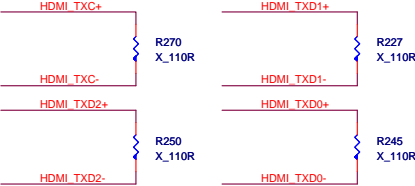
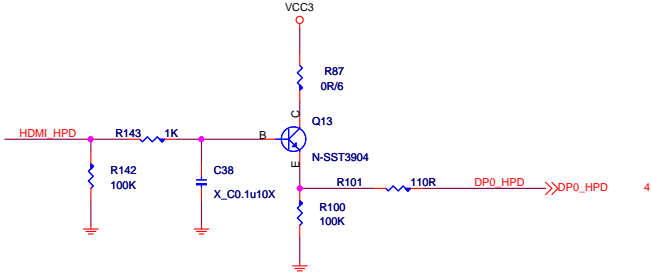
Near Front



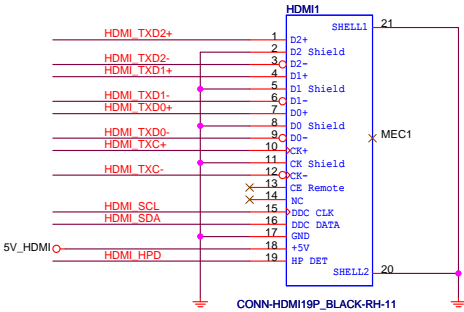
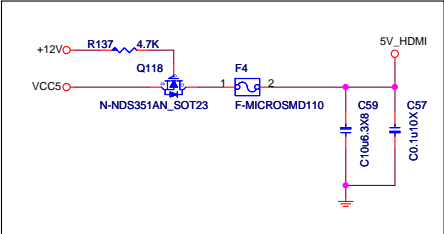
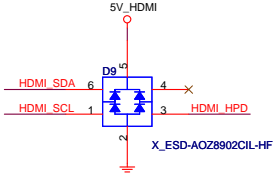
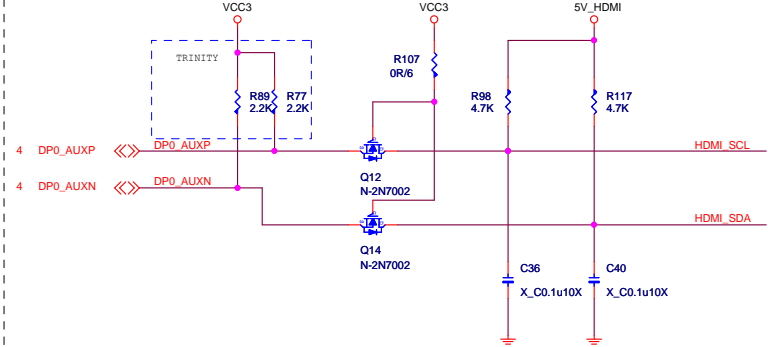
HDMI CONNECTOR



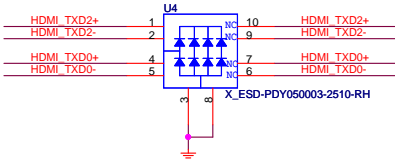
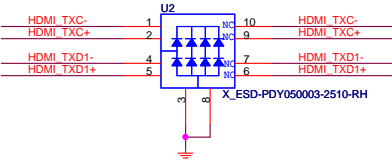
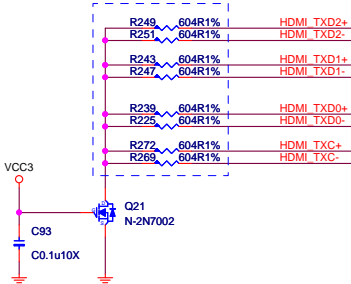
HDMI
DP0_TXP/N0 Data2
DP0_TXP/N1 Data1
DP0_TXP/N2 Data0
DP0_TXP/N3 Clock



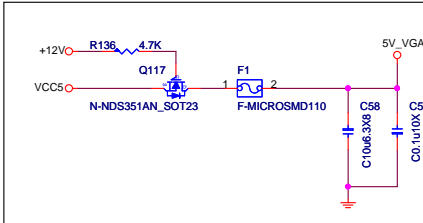
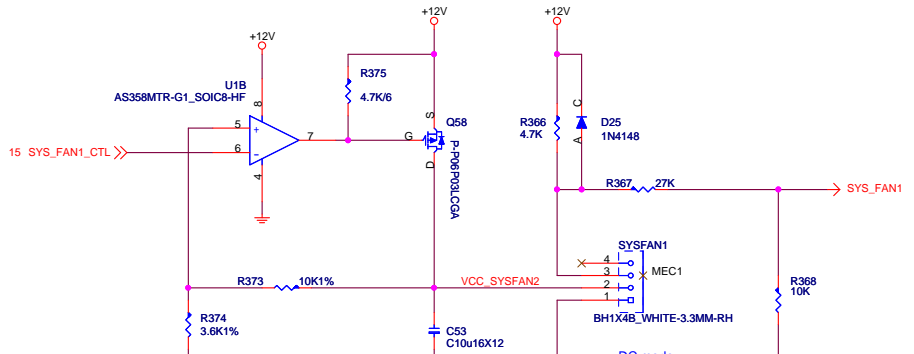
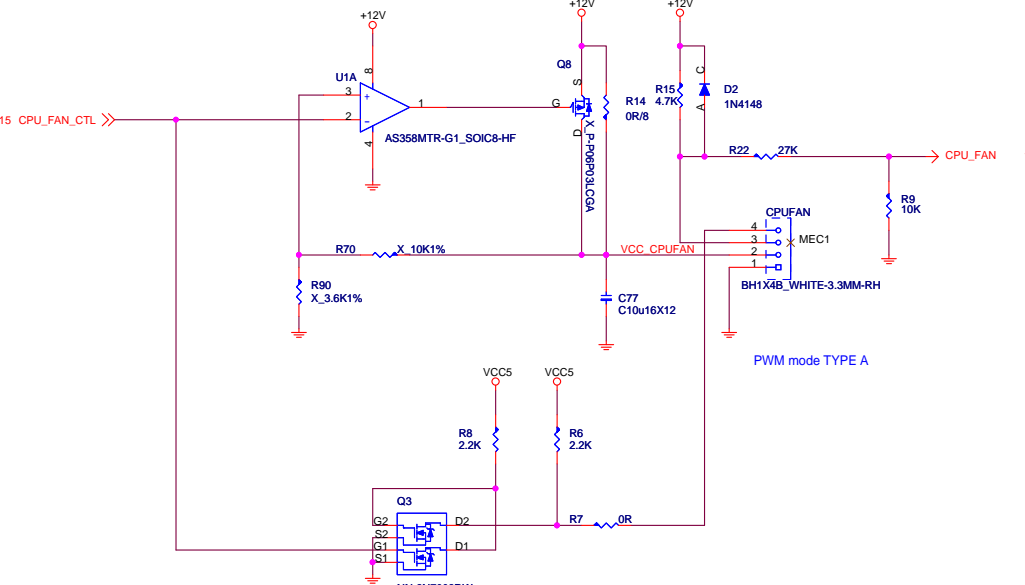
LEVEL SHIFT using I2C Repeater



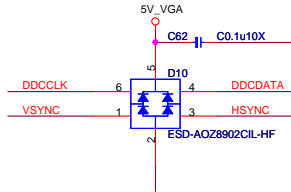
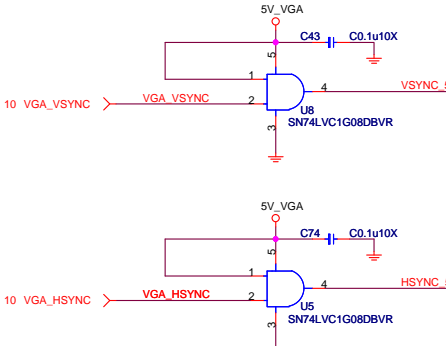
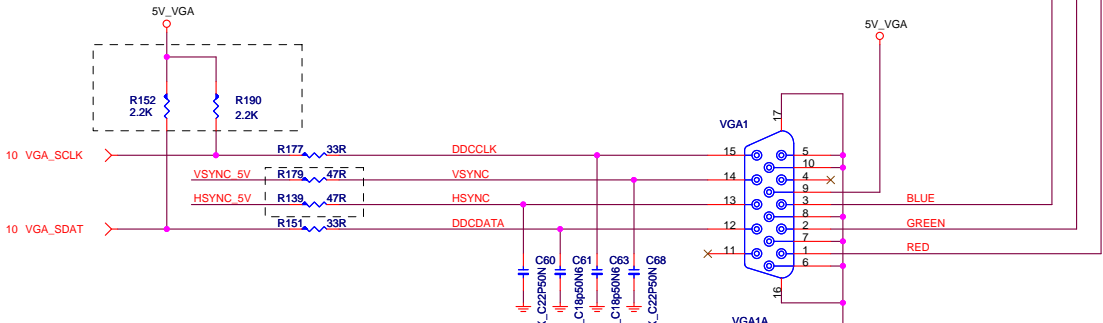
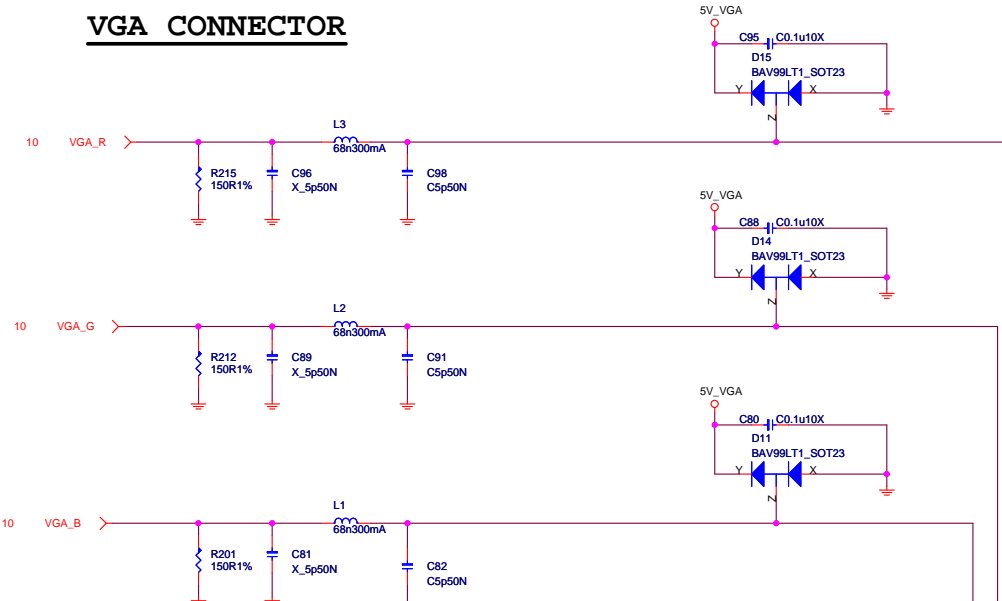
03/20 Change HDMI (TMDS) terminations from 715ohm to 604ohm

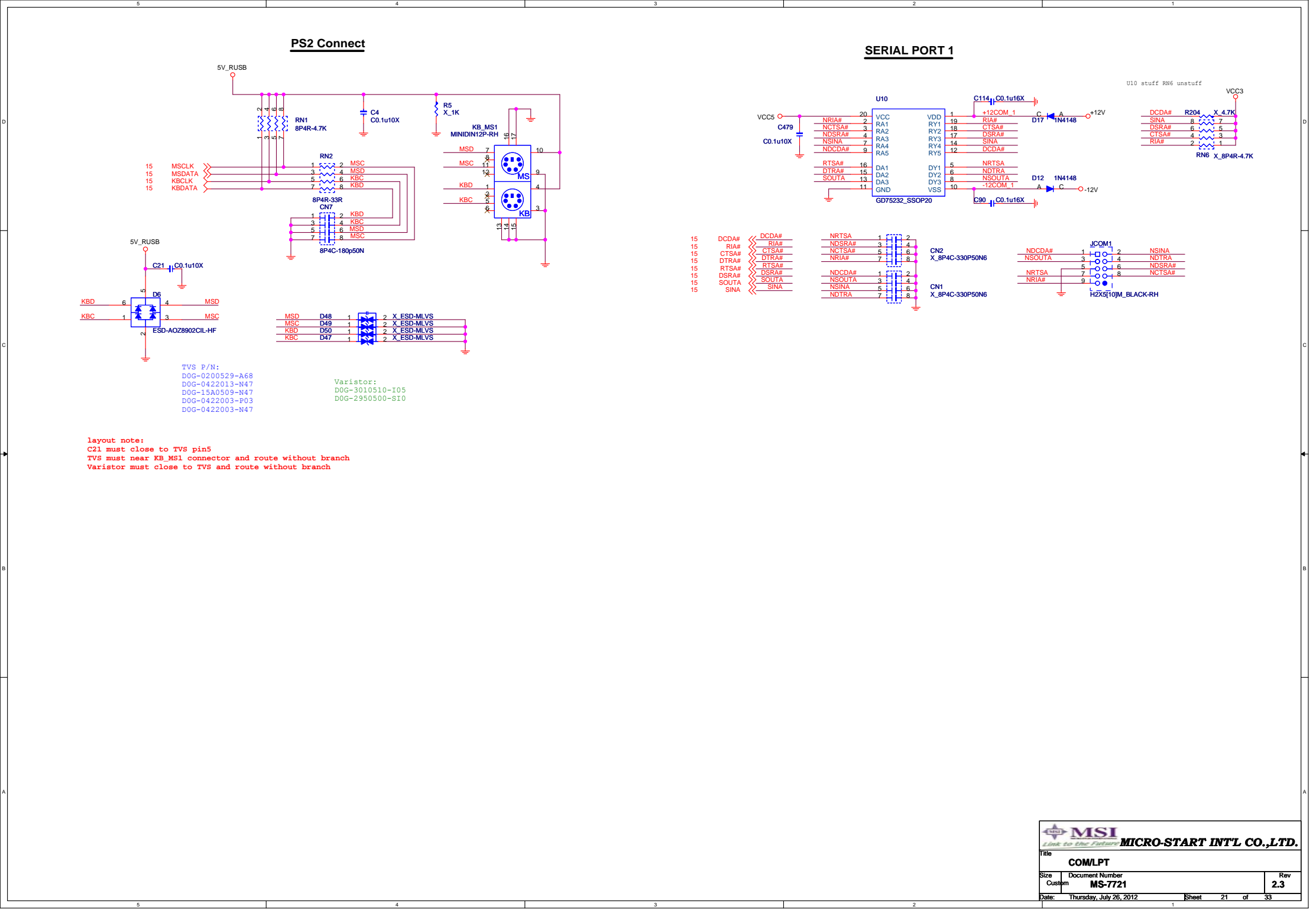


FAN

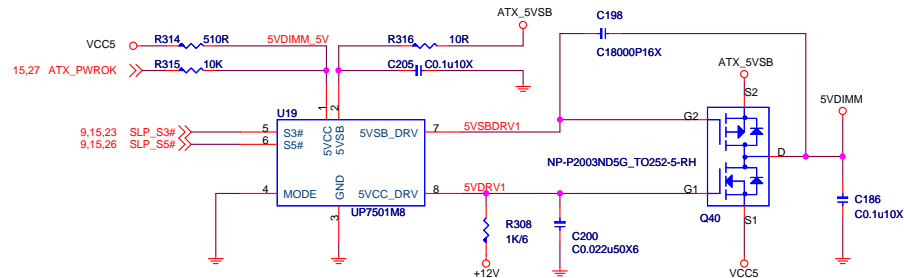


VGA CONNECTOR



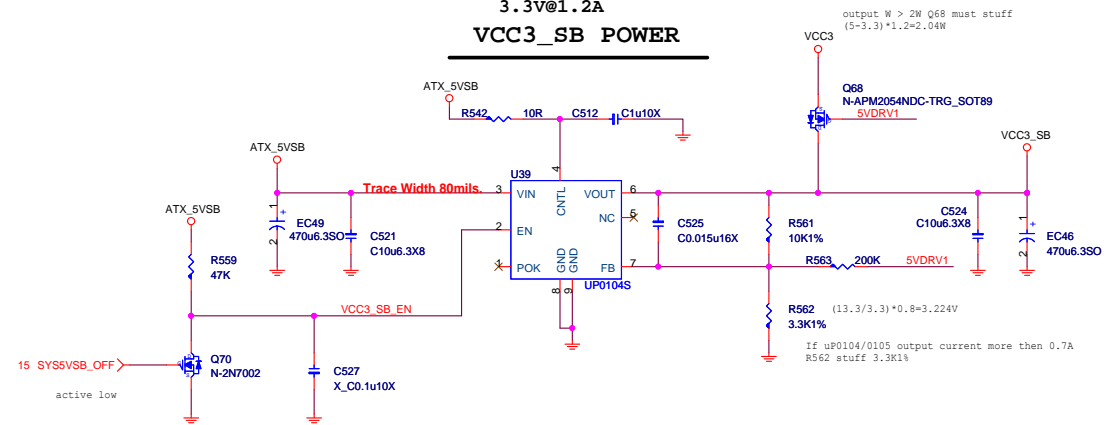
[illegible][illegible][illegible]

5VDIMM FOR DDR

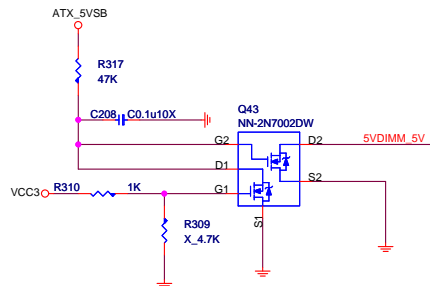


D03-020030B-N03 add avl D03-P19030B-N03

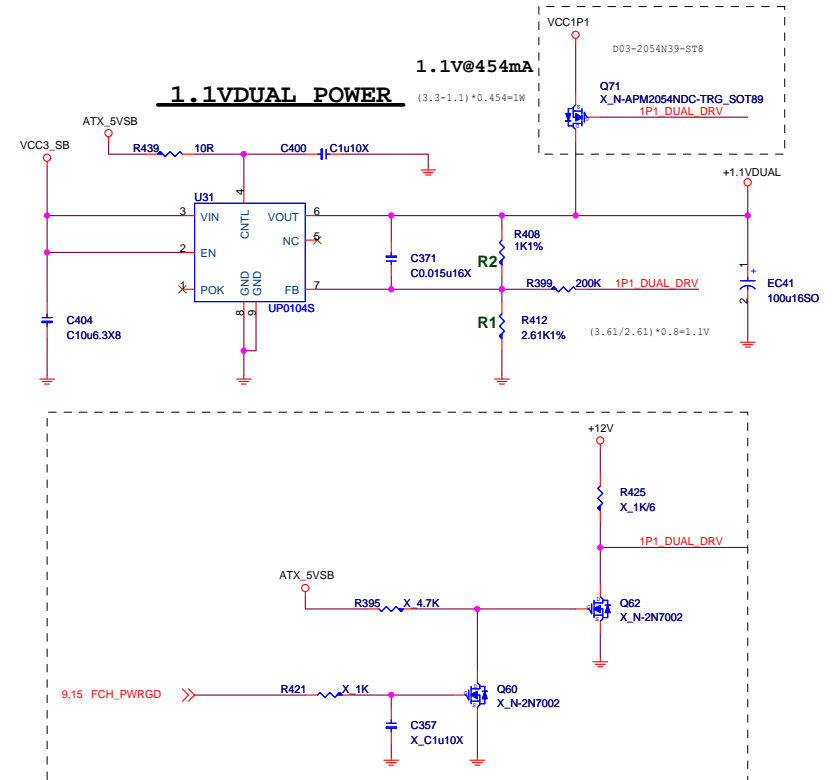
3.3V@1.2A
VCC3_SB POWER



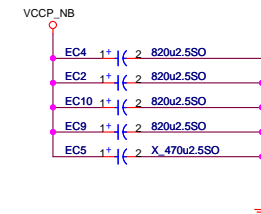
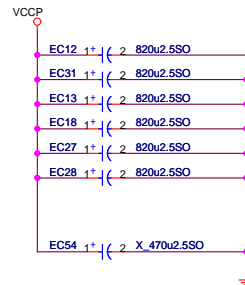
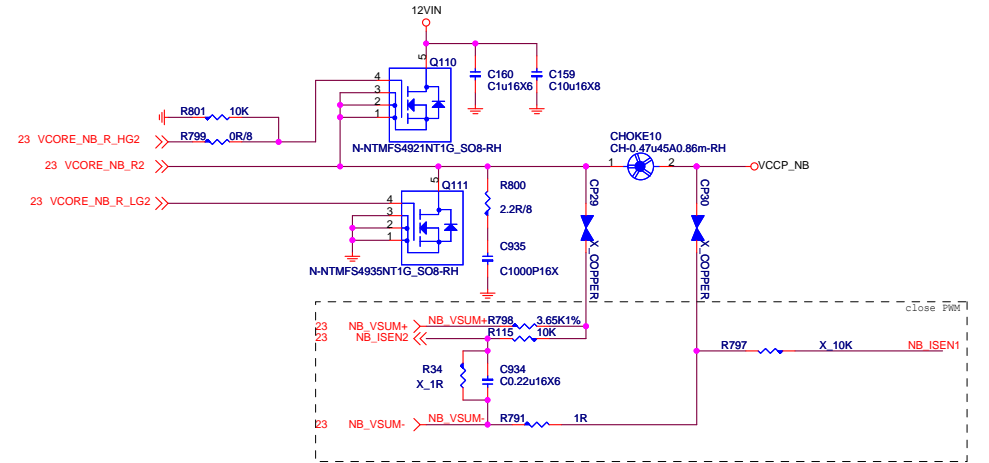
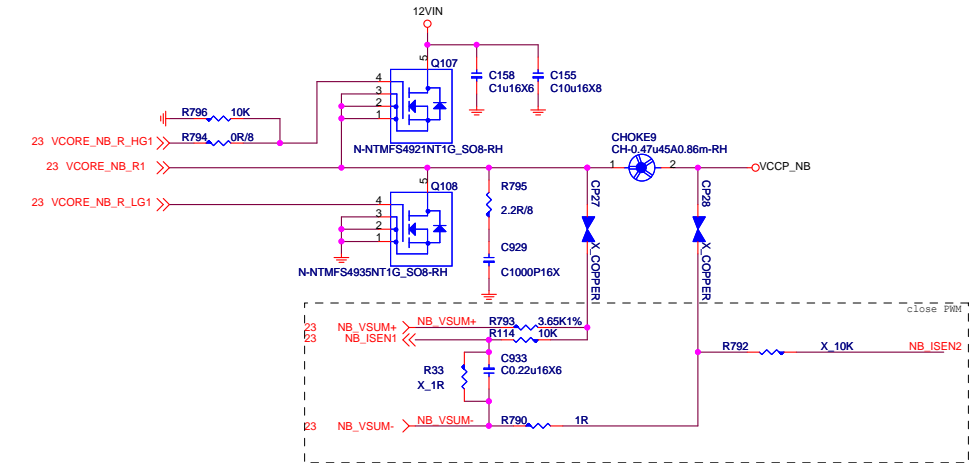
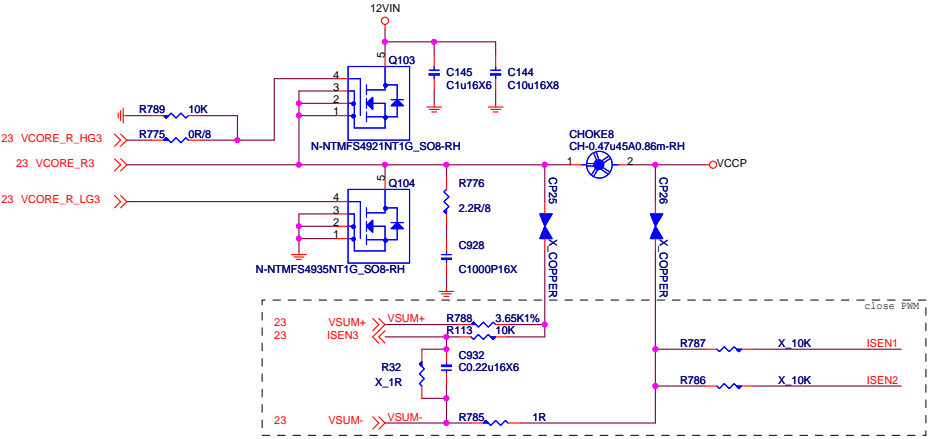
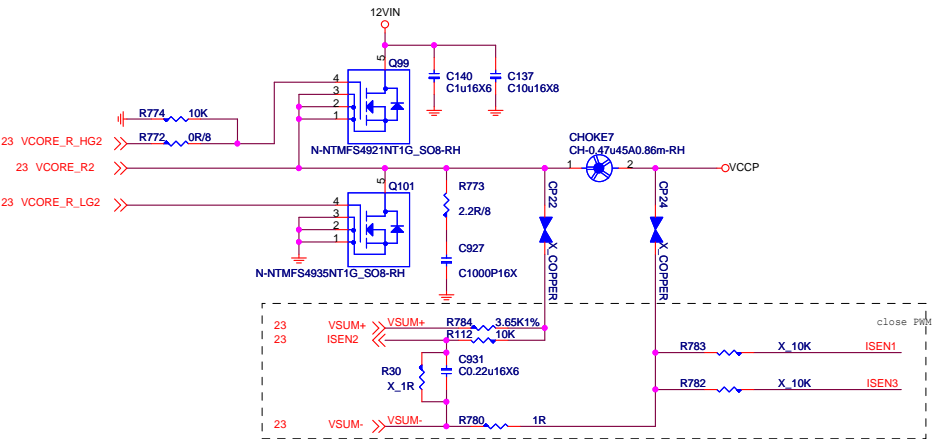
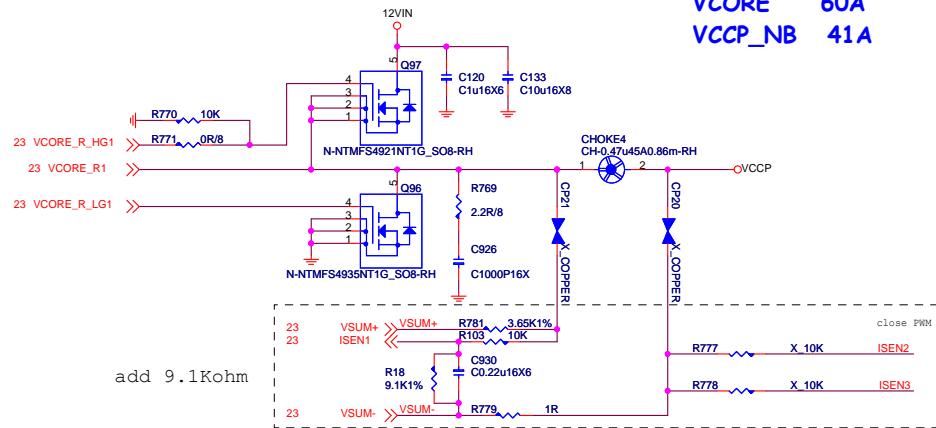
For special PSU sequence



1.1VDUAL POWER

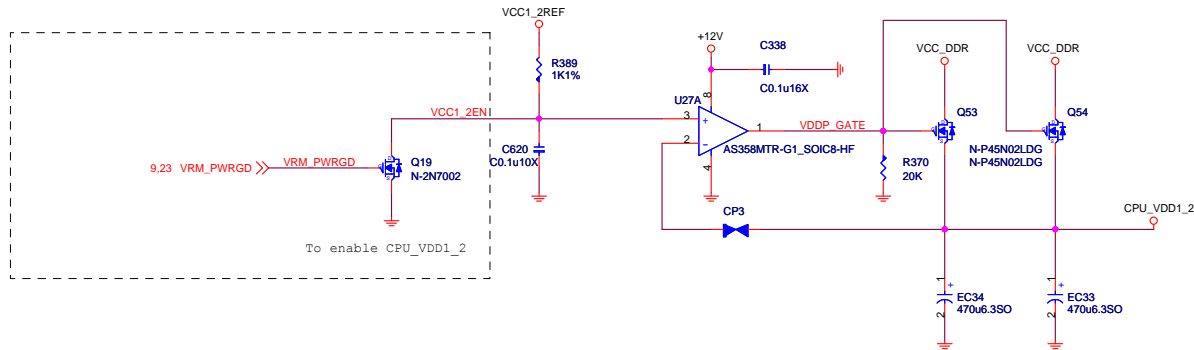


VCORE 60A
VCCP_NB 41A



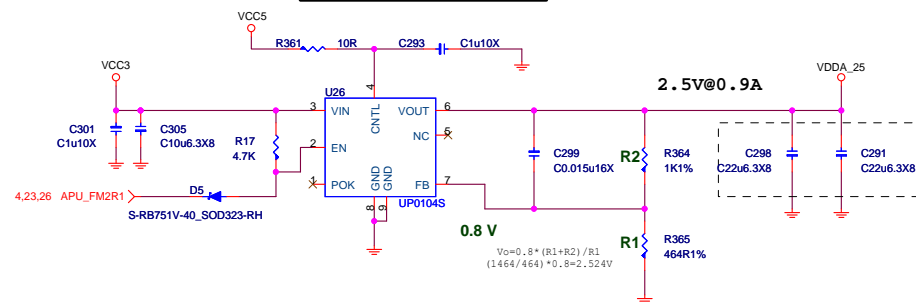
1.2 V@6A+4A

1.2 V@6A+4A

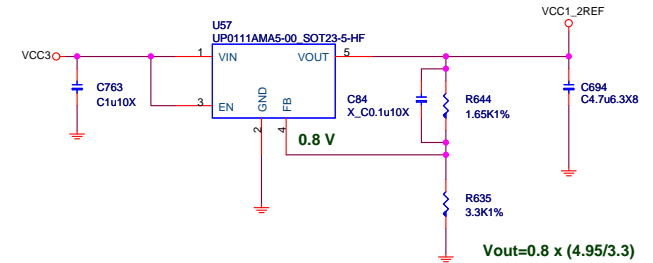


VDDA_25 0.9A

VDDA_25 0.9A



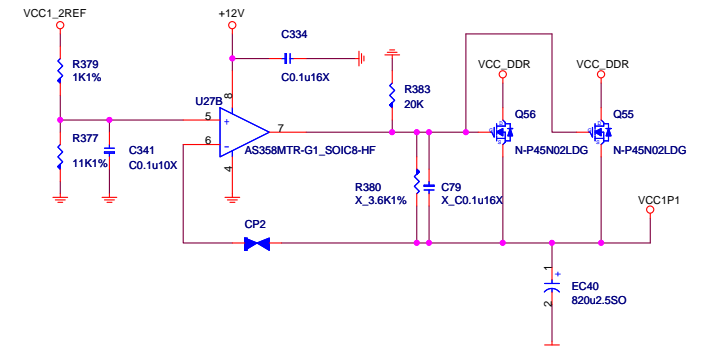
VCC1_2REF



VCC1P1 4.4A

VCC1P1 POWER

1.1V@4.4A



D



B

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A

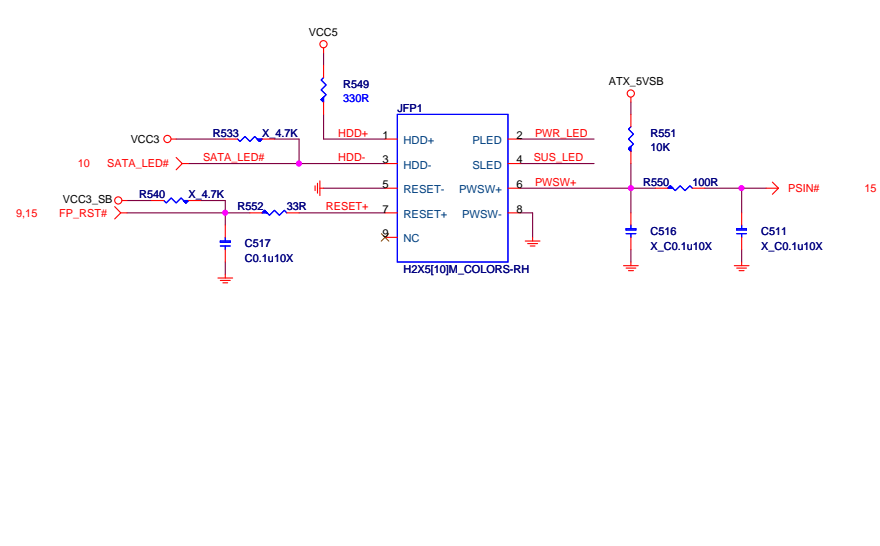
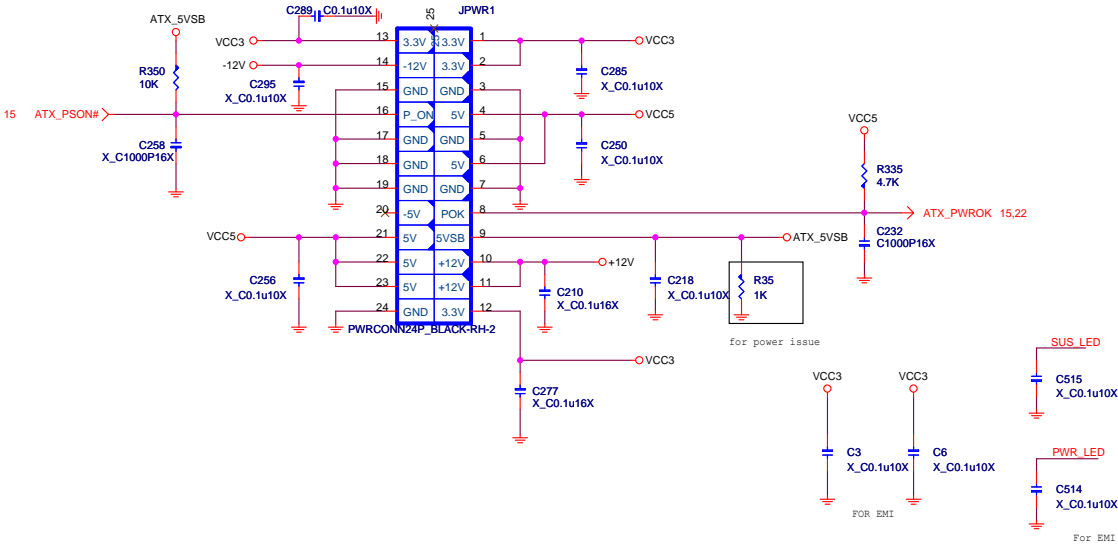


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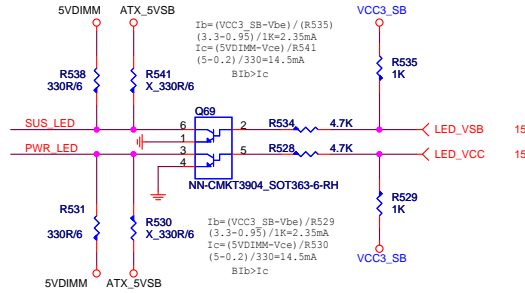
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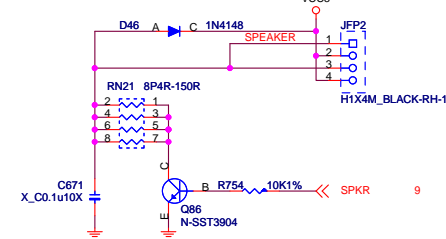
ATX CONNECTOR



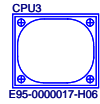
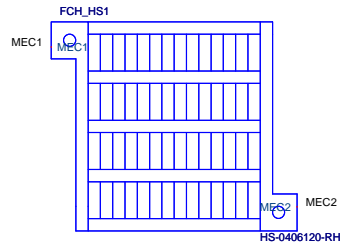
LED (for Fintek 71868)



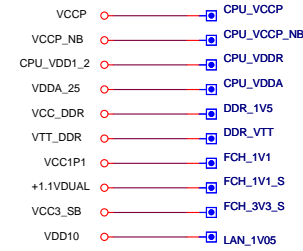
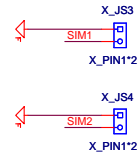
BUZZER



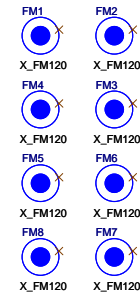
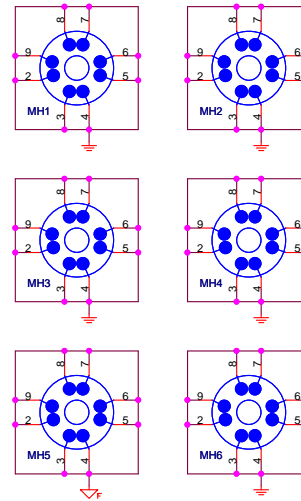
HEAT SINK



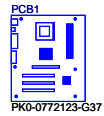
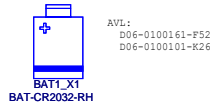
Simulation



Optics Orientation Holes



MANUAL PART



PK0-0772123-G37, 精成, 23, 寶安恩斯邁廠 (MSIS)
PK0-0772123-E48, 競華, 23, 寶安恩斯邁廠 (MSIS)

MK1
G51-M1SPC81-F32
G51-M1SPC81-Q13

UEFI1
G51-M1SPXXA-A09

HDMI_LAB
Y01-RHDMI03-000